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10/821,182	04/09/2004	Jeong-Hoon Choi	P-0670	8416

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EXAMINER	
CHURNET, DARGAYE H	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,182	CHOI, JEONG-HOON	
	Examiner	Art Unit	
	DARGAYE H. CHURNET	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11,13-18,22 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-11,13-18,22 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/29/08 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5, 6, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Jayakumar et al. (cited 7,031,312).

For claim 1, Jayakumar discloses a method for managing ATM resources, comprising: passing an ATM cell (see fig. 3, ATM cell) received by an ATM switch (see fig. 2, ATM Node 235) to a cell processing circuit (see fig. 2, Egress LSR 250), said passing including adding an alpha Byte of routing information (see col. 4, lines 6-9, VC

label) to a header of the ATM cell (see col. 4, lines 6-9, prepending the VC label to the ATM cell); removing the routing information (see col. 4, lines 12-15, wherein the VC label is removed) added to the ATM cell after processing by the cell processing circuit (see col. 4, lines 12-15, wherein the VC label is removed at the egress LSR 250); and routing the ATM cell to a destination based on the removed routing information (see col. 4, lines 12-15, routing the ATM cell to the destination based on the removed VC label), wherein the routing information is added after the ATM cell passes through the ATM switch (see col. 4, lines 4-9, wherein ingress LSR 240 prepends the VC label after it has passed through ATM node 235) and wherein the ATM cell is routed along a signal path that bypasses the ATM switch after the routing information is removed (see fig. 2, wherein the ATM cell bypasses the ATM node 235 after the VC label is removed at egress LSR 250).

For claim 2, Jayakumar discloses a method of switching an asynchronous transfer mode (ATM) cell having a payload portion and a header portion (see fig. 3, ATM cell) comprising: passing the ATM cell (see fig. 3, ATM cell) received through an ATM switch (see fig. 2, ATM Node 235) to a cell processing circuit (see fig. 2, Egress LSR 250), said passing including adding a destination information field (see col. 4, lines 6-9, VC label) to the header portion of the ATM cell (see col. 4, lines 6-9, prepending the VC label to the ATM cell); processing the ATM cell (see fig. 2, Egress LSR 250 is cell processing circuit); and forwarding the ATM cell to a destination after the destination information field is removed (see col. 4, lines 12-15, routing the ATM cell to the

destination based on the removed VC label), wherein the ATM cell is forwarded to said destination along a signal path that bypasses the ATM switch (see fig. 2, wherein the ATM cell bypasses the ATM node 235 after the VC label is removed at egress LSR 250) and wherein the destination information field is added to the header portion by the ATM switch or a circuit located between the ATM switch and the cell processing circuit (see col. 4, lines 4-9, wherein ingress LSR 240 prepends the VC label after it has passed through ATM node 235).

For claim 5, Jayakumar discloses a method of processing an asynchronous transfer mode (ATM) cell (see fig. 3, ATM cell) comprising: switching a received ATM cell (see fig. 3, ATM cell) through an ATM switch (see fig. 2, ATM Node 235); adding routing information (see col. 4, lines 6-9, VC label) in a header of the ATM cell that has been switched (see col. 4, lines 6-9, prepending the VC label to the ATM cell); and forwarding the ATM cell according to the added routing information to a destination based on the routing information added to the header of the ATM cell (see col. 4, lines 12-15, routing the ATM cell to the destination based on the removed VC label), wherein routing information is removed from the ATM cell (see col. 4, lines 12-15, wherein the VC label is removed) and the ATM cell is forwarded to the destination along a signal path that bypasses the ATM switch see fig. 2, wherein the ATM cell bypasses the ATM node 235 after the VC label is removed at egress LSR 250), and wherein the destination information field is added to the header portion by the ATM switch or a circuit located between the ATM switch and the cell processing circuit (see col. 4, lines

4-9, wherein ingress LSR 240 prepends the VC label after it has passed through ATM node 235).

For claim 3, Jayakumar discloses the ATM cell during processing has (53+alpha) bytes, and alpha corresponds to a size of the information field (see fig. 3, wherein the ATM cell inherently comprises 53 bytes and the alpha extra bytes are the MPLS stack including VC label 310).

For claim 6, Jayakumar discloses the received ATM cell has a size of 53 bytes (see fig. 3, wherein the ATM cell is inherently 53 bytes).

For claim 9, Jayakumar discloses processing the ATM cell before forwarding (see fig. 2, wherein egress LSR 250 processes the cell before forwarding to ATM network 215).

Claim Rejections - 35 USC § 103

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 8, 10, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jayakumar in view of Smith (cited 6,349,097).

For claim 7, Jayakumar fails to disclose the added routing information has a size of 1 byte. Smith from the same or similar fields of endeavor teaches the added routing information has a size of 1 byte (see col. 11, lines 62-66, wherein the routing tag is a single byte). Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to incorporate the elements above stated by Smith in the network of Jayakumar. The method taught by Smith is modified/implemented into the network of Jayakumar by using a routing tag with the size of 1 byte. The motivation for the added routing information having a size of 1 byte is to not add too much overhead to the packet size.

For claim 8, Jayakumar discloses the forwarded ATM cell has a size of 53 bytes, after the 1 byte routing information has been removed (see col. 14, lines 26-28, wherein the routing tag is removed, and then output to the destination, so the destination receives the original ATM cell with a size of 53 bytes).

For claim 10, Smith teaches changing of an ATM adaptation layer (AAL) type or a changing of payload information (see fig. 5, wherein the payload information is changed). Claim 22 is rejected for similar reasons.

For claim 23, Jayakumar discloses the routing information included in the alpha Byte identifies one of the following as a destination of the ATM cell: one of a plurality of physical connections or a loop-back path of a network (see fig. 2, wherein the VC label is a destination to physical connections to ATM network 215).

5. Claims 11 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Jayakumar.

For claim 11, the admitted prior art discloses an asynchronous transfer mode (ATM) cell switching system comprising (see fig. 1): a first memory to receive and store an ATM cell to be handled (see fig. 1, Queue3); a cell switching unit to receive the ATM cell stored in the first memory and to assign an appropriate path for the ATM cell to be forwarded (see fig. 1, Cell Switching Unit); a second memory to receive and store the ATM cell having the appropriate path assigned thereto from the cell switching unit (see fig. 1, Queue1); a cell processor to receive and process the ATM cell from the second memory (see fig. 1, Cell Processing Unit); and a third memory to receive and store the ATM cell processed by the cell processor (see fig. 1, Queue2). The admitted prior art fails to disclose outputting the ATM cell without going through the cell switching unit. Jayakumar from the same or similar fields of endeavor teaches outputting the ATM cell

without going through the cell switching unit (see fig. 2, wherein the Ingress LSR 240 is the cell switching unit and the cell is passed to Egress LSR 250 without going back through Ingress LSR 240). Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to incorporate the elements above stated by Jayakumar in the network of the admitted prior art. The method taught by Jayakumar is modified/implemented into the network of the admitted prior art by avoiding looping and transmitting the cell directly to the destination. The motivation for outputting the ATM cell without going through the cell switching unit is to avoid looping and unnecessarily transmitting a cell through the same switching unit multiple times.

For claim 13, the admitted prior art discloses the cell switching unit provides an output to a physical layer and to a loop back, or an output for further processing (see fig. 1, wherein the outputs from the cell switching unit is a physical layer, loop back, and further processing).

For claim 14, Jayakumar teaches the cell switching unit adds an end destination field in a header of the ATM cell (see col. 4, lines 6-9, wherein the ingress LSR 240 prepends the VC label to the ATM cell).

For claim 15, Jayakumar teaches the added end destination field is maintained as the ATM cell passes through the second memory, the cell processor and third

memory (see fig. 2, wherein ingress LSR 240 adds the destination field and passes to the egress LSR 250 which has a second memory, cell processor, and third memory).

For claim 16, Jayakumar teaches the third memory outputs the ATM cell directly to a physical layer or to a loop back in accordance with information included in the end destination field (see fig. 2, wherein the memory within egress LSR 250 transmits the cell to a physical layer within ATM network 215).

For claim 17, Jayakumar teaches the cell switching unit requires a one virtual path identifier/virtual channel identifier (VPI/VCI) and one type of routing information for any received ATM cell (see fig. 3, wherein an ATM cell inherently requires VPI/VCI and routing information).

6. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Jayakumar, as applied to claim 11 above, and further in view of Smith.

For claim 18, the admitted prior art in view of Jayakumar fails to disclose the cell processor processes the received ATM cell by changing an ATM adaptation layer (AAL) type or by changing payload information. Smith from the same or similar fields of endeavor teaches the cell processor processes the received ATM cell by changing an ATM adaptation layer (AAL) type or by changing payload information (see fig. 5, wherein the payload information is changed). Thus, it would have been obvious to the

person of ordinary skill in the art at the time of the invention to incorporate the elements above stated by Smith in the network of the admitted prior art in view of Jayakumar. The method taught by Smith is modified/implemented into the network of the admitted prior art in view of Jayakumar by changing payload information of the ATM cell during processing. The motivation for the cell processor processes the received ATM cell by changing an ATM adaptation layer (AAL) type or by changing payload information is to update the ATM cell.

Response to Arguments

7. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dargaye H. Churnet whose telephone number is 571-270-1417. The examiner can normally be reached on Monday-Friday from 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chirag Shah can be reached on 571-272-3144. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dargaye H Churnet/
Examiner, Art Unit 2419

/Chirag G Shah/

Supervisory Patent Examiner, Art Unit 2419